Tushar Pathak

Phone: +1 (718) 413-9793 | Email: tushar.p@nyu.edu | LinkedIn: linkedin.com/in/tushar-pathak | GitHub: github.com/tusharpathaknyu

Education

New York University — New York, USA
M.S. Computer Engineering (Graduate Scholarship Recipient) — *January 2024 - December 2025*

Birla Institute of Technology and Science (BITS) Pilani — Hyderabad, India
B.E. Electrical and Electronics Engineering — *August 2019 - July 2023*

Work Experience

Texas Instruments — Bangalore, India
Applications Intern — *January 2023 - July 2023*

- Benchmarked competitor 65W chargers featuring Quasi-Resonant (QR) flyback converters and **Gallium Nitride (GaN)** based MOSFETs in a high voltage laboratory.
- Spearheaded hardware enhancements based on benchmarking insights, contributing to a 15% improvement in reliability and a 25% reduction in support tickets for a $2M+ product line.
- Devised a custom **Printed Circuit Board (PCB)** using Altium Designer for DC/DC characterization, facilitating prototype evaluations and reducing hardware testing cycles by 30%.
- Realized design modifications resulting in a 5% increase in charger efficiency and 12% cost reduction; testing hardware is now utilized across 15 global labs.

Dreamline AI — Remote
Software Engineer — *August 2025 - Present*

- Architected cleantech web platforms using React/Next.js and TypeScript, achieving a 35% user engagement increase and maintaining 99.9% uptime via Supabase synchronization.

Xarvis Intelligent Systems Lab — Pune, India
Software Engineering Intern — *May 2021 - July 2021*

- Synthesized a multi-tenant backend using Spring Boot for 50,000+ users and implemented a database-per-tenant strategy with MySQL, reducing deployment time by 40%.

Projects

PowerElecLLM: Hardware Design Benchmark & Fine-Tuning — Link

- Pioneered an evaluation framework testing 4 **Large Language Models (LLMs)** on 650 problems; fine-tuned GPT-4o, achieving a 25% accuracy rate (17% improvement over baseline).
- Mechanized an ngspice-based SPICE Evaluator to verify designs (Duty Cycle, L, C) for 10 topologies including Flyback, Full-Bridge, Buck, and SEPIC converters.
- Orchestrated a transient simulation engine in Python to measure steady-state output voltage from waveforms, ensuring designs meet target voltage within a 10% tolerance threshold.

OhmAI: RAG-Based Circuit Design Agent — Link

- Streamlined a Python-based LTSpice interface to coordinate 100+ iterative simulations, enabling the agent to autonomously discover optimal efficiency setpoints for Buck/Boost topologies.
- Formulated a **Retrieval-Augmented Generation (RAG)** pipeline using LangChain and FAISS to query 1,000+ technical notes, reducing design research time by 60%.
- Systematized a structured parsing system for electrical characteristics, achieving 92% accuracy in automated component comparisons for power stage optimization.

Home Automation Controller PCB

- Constructed a 2-layer **Printed Circuit Board (PCB)** in Altium Designer for switching 4 AC relays and 48V DC loads, reducing board area by 30% and material costs by 15%.
- Refined the layout for 10A high-current paths using thermal modeling, ensuring zero violations in verification and maintaining temperature rise below 20 degrees Celsius.

Technical Skills

Power Electronics: DC/DC Converters, GaN MOSFETs, **Electromagnetic Interference (EMI)** and **Compatibility (EMC)** Filtering, Loop Compensation, Magnetics Design.
Hardware & EDA Tools: Altium Designer, ngspice, LTSpice, PSpice, MATLAB/Simulink, Verilog, Xilinx Vivado, AutoCAD, PCB Layout (High Power/High Speed).
AI & Software: Python (SciPy, NumPy), LLM Fine-tuning (QLoRA, Unsloth), LangChain (RAG), FAISS, PyTorch, React/Next.js, TypeScript, Spring Boot, MySQL, Docker, Git.