Tushar Pathak

Phone: +1 (718) 413-9793 | Email: tushar.p@nyu.edu | LinkedIn: linkedin.com/in/tushar-pathak | GitHub: github.com/tusharpathaknyu

Education

New York University — New York, USA
M.S. Computer Engineering (Graduate Scholarship Recipient) — *January 2024 - December 2025*

Birla Institute of Technology and Science (BITS) Pilani — Hyderabad, India
B.E. Electrical and Electronics Engineering — *August 2019 - July 2023*

Work Experience

Texas Instruments — Bangalore, India
Applications Intern — *January 2023 - July 2023*

- Conducted competitive benchmarking of 65W chargers using **Quasi-Resonant (QR)** flyback converters and **Gallium Nitride (GaN)** based MOSFETs in a high voltage lab.
- Synthesized hardware enhancements based on benchmarking insights, contributing to a 15% improvement in reliability for a $2M+ product line.
- Devised a custom **Printed Circuit Board (PCB)** using Altium Designer for internal DC/DC characterization, reducing hardware testing cycles by 30%.
- Realized design modifications resulting in a 5% increase in charger efficiency and 12% cost reduction; hardware is now utilized across 15 global labs.

Dreamline AI — Remote
Software Engineer — *August 2025 - Present*

- Architected cleantech web platforms using React/Next.js and TypeScript, achieving a 35% user engagement increase and maintaining 99.9% uptime via Supabase.

Xarvis Intelligent Systems Lab — Pune, India
Software Engineering Intern — *May 2021 - July 2021*

- Constructed a multi-tenant backend using Spring Boot for 50,000+ users, reducing deployment time by 40% via a database-per-tenant strategy.

Projects

UVMForge: AI-Powered Verification Testbench Generator — Link

- Pioneered an AI framework that transforms natural language specifications into production-ready **Universal Verification Methodology (UVM)** testbenches in approximately 5 seconds.
- Engineered **RTL-aware generation** capabilities for exact port matching and protocol detection (APB, AXI4-Lite, SPI, I2C, UART) from SystemVerilog source files.
- Mechanized a **SystemVerilog Assertion (SVA)** generator that produces 50+ assertions for protocol compliance, handshake checks, and Finite State Machine (FSM) properties.
- Orchestrated a coverage gap analysis tool that prioritizes uncovered bins and generates targeted UVM sequences to reach 100% functional coverage goals.

5-Stage Pipelined RISC-V Processor — Link

- Spearheaded the design of a **Reduced Instruction Set Computer (RISC-V)** processor in Verilog, achieving a 25% performance gain through parallel pipeline execution.
- Implemented data and control hazard detection logic with data forwarding, reducing pipeline stalls by 30% and enhancing cycle efficiency by 18%.
- Validated the core functionality using SystemVerilog testbenches, ensuring compliance with arithmetic and logic instruction set specifications.

OhmAI: RAG-Based Circuit Verification Agent — Link

- Streamlined a Python-based LTSpice interface to coordinate 100+ iterative simulations, enabling the agent to autonomously discover optimal efficiency setpoints.
- Formulated a **Retrieval-Augmented Generation (RAG)** pipeline using LangChain and FAISS to query technical notes, reducing design verification research time by 60%.
- Pioneered a structured parsing system for electrical characteristics, achieving 92% accuracy in automated component comparisons for power stage optimization.

Technical Skills

Verification Methodologies: Universal Verification Methodology (UVM), **SystemVerilog Assertion (SVA)**, Functional Coverage, Code Coverage, Scoreboarding, Constraints.
Hardware Description Languages: SystemVerilog, Verilog, VHDL, RISC-V Architecture.
Hardware & EDA Tools: Xilinx Vivado, Altium Designer, LTSpice, ngspice, Cadence Virtuoso, MATLAB/Simulink, PCB Layout.
Programming & AI: Python (SciPy, NumPy), C++, LLM Fine-tuning (QLoRA, Unsloth), LangChain (RAG), React/Next.js, Docker, Git.